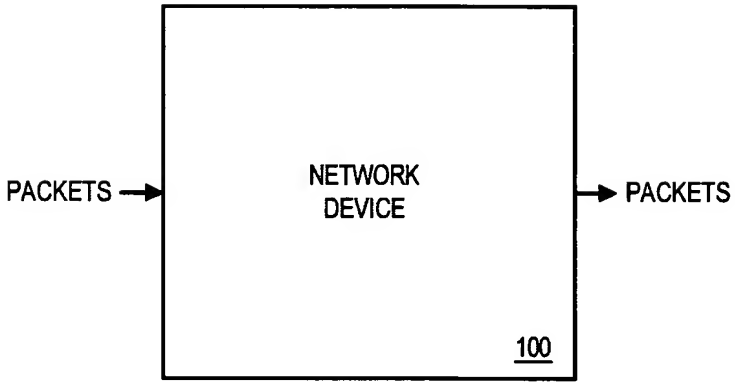

FIG. 1

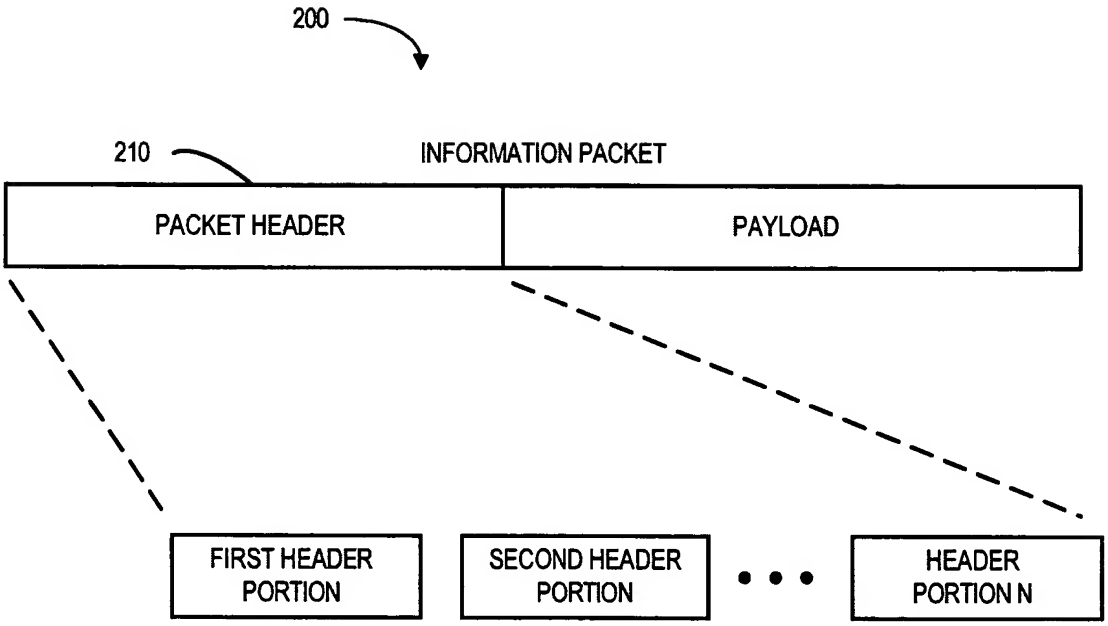
200
210
INFORMATION PACKET
PACKET HEADER
PAYLOAD
FIRST HEADER PORTION
SECOND HEADER PORTION
HEADER PORTION N

FIG. 2

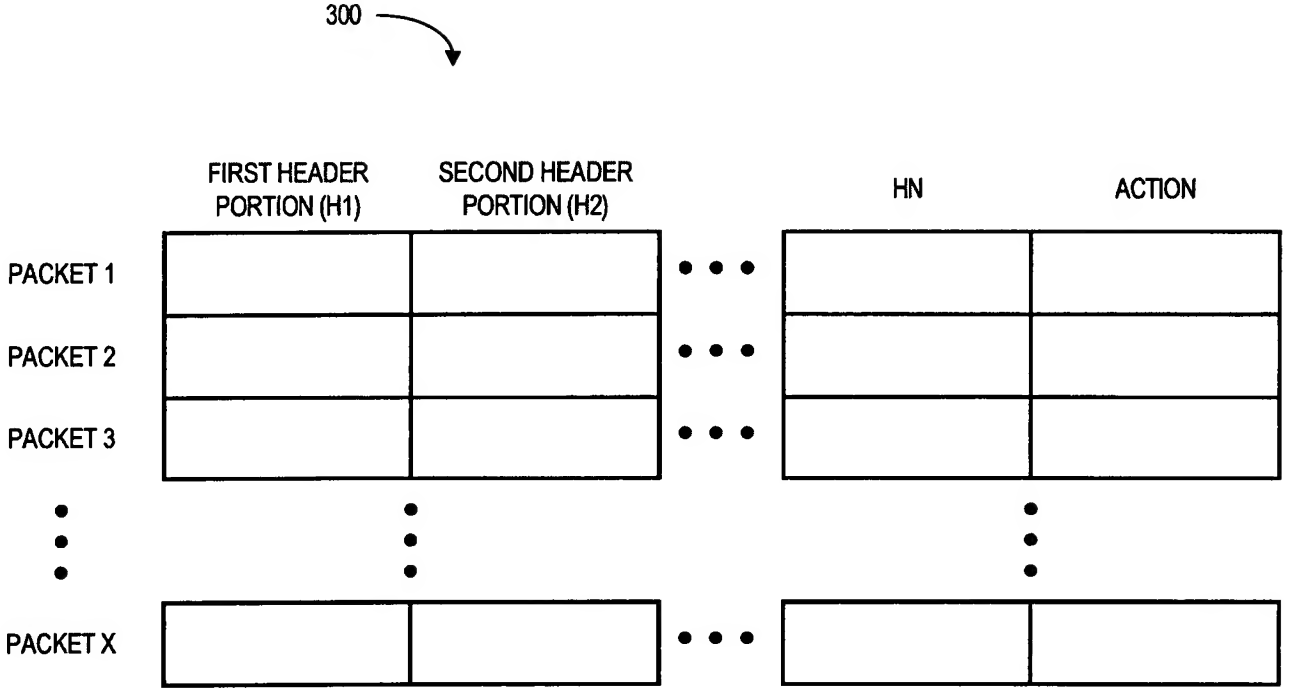
300
FIRST HEADER PORTION (H1)
SECOND HEADER PORTION (H2)
HN
ACTION
PACKET 1
PACKET 2
PACKET 3
PACKET X

FIG. 3

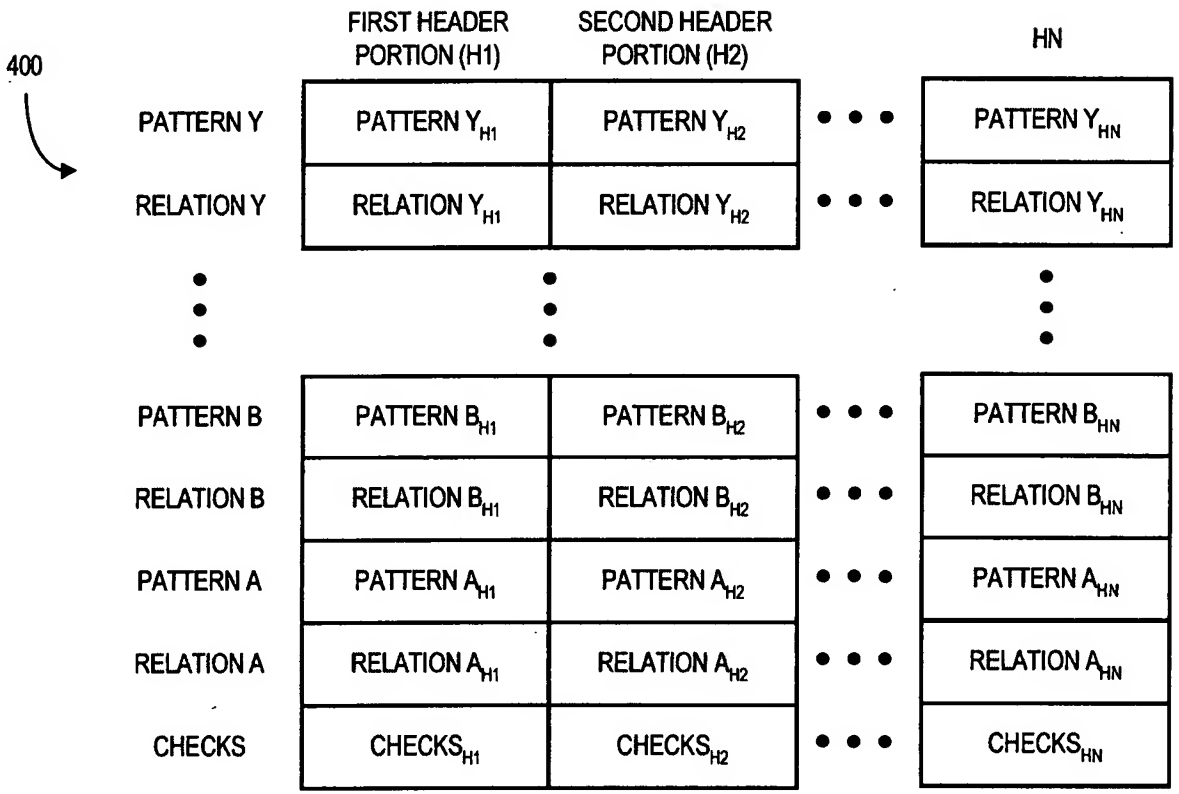
400
FIRST HEADER PORTION (H1)
SECOND HEADER PORTION (H2)
HN
PATTERN Y
PATTERN Y_{H1}
PATTERN Y_{H2}
PATTERN Y_{HN}
RELATION Y
RELATION Y_{H1}
RELATION Y_{H2}
RELATION Y_{HN}
PATTERN B
PATTERN B_{H1}
PATTERN B_{H2}
PATTERN B_{HN}
RELATION B
RELATION B_{H1}
RELATION B_{H2}
RELATION B_{HN}
PATTERN A
PATTERN A_{H1}
PATTERN A_{H2}
PATTERN A_{HN}
RELATION A
RELATION A_{H1}
RELATION A_{H2}
RELATION A_{HN}
CHECKS
$CHECKS_{H1}$
$CHECKS_{H2}$
$CHECKS_{HN}$

FIG. 4

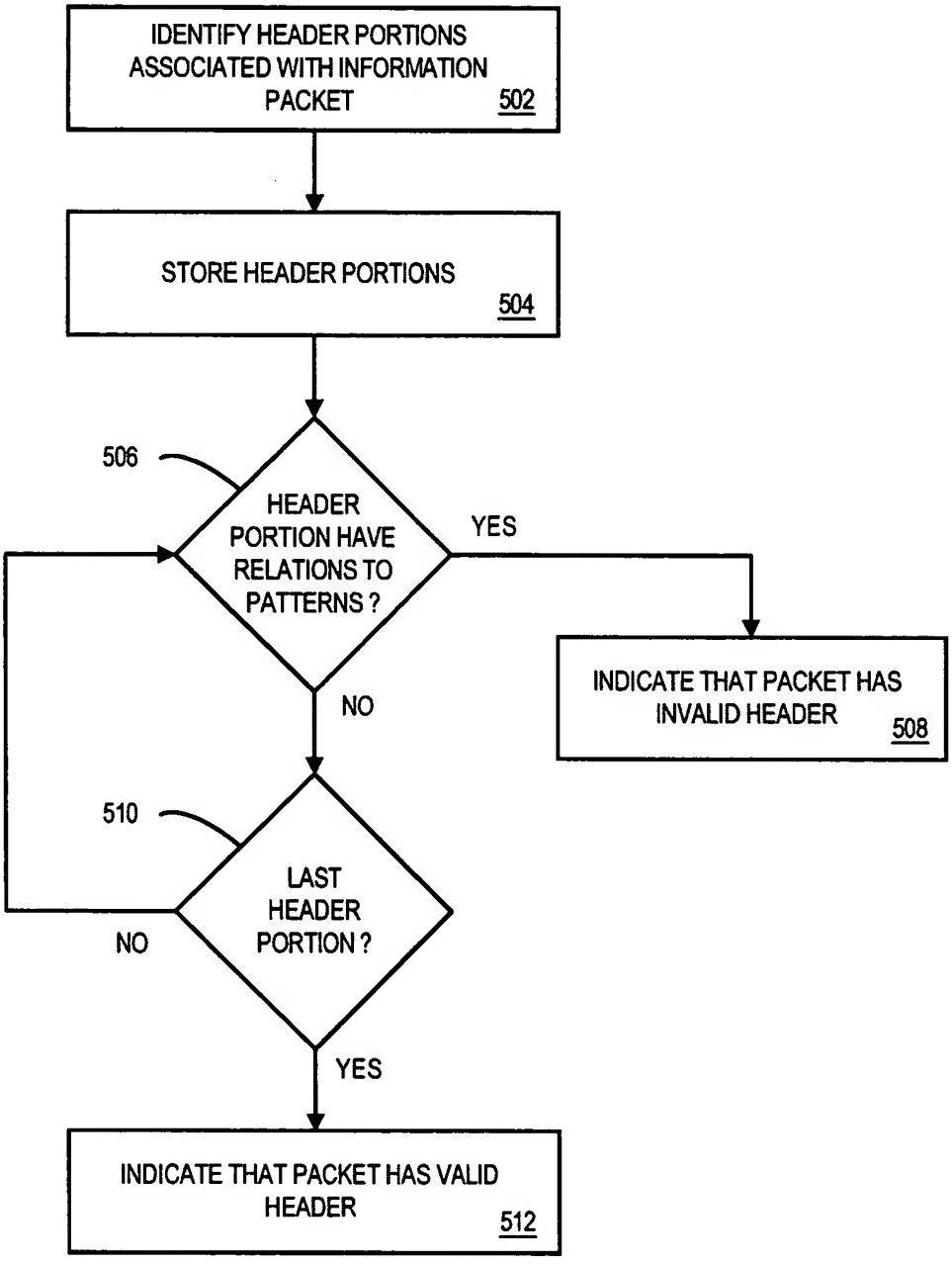
IDENTIFY HEADER PORTIONS ASSOCIATED WITH INFORMATION PACKET
502
STORE HEADER PORTIONS
504
506
HEADER PORTION HAVE RELATIONS TO PATTERNS ?
YES
INDICATE THAT PACKET HAS INVALID HEADER
508
NO
510
LAST HEADER PORTION ?
NO
YES
INDICATE THAT PACKET HAS VALID HEADER
512

FIG. 5

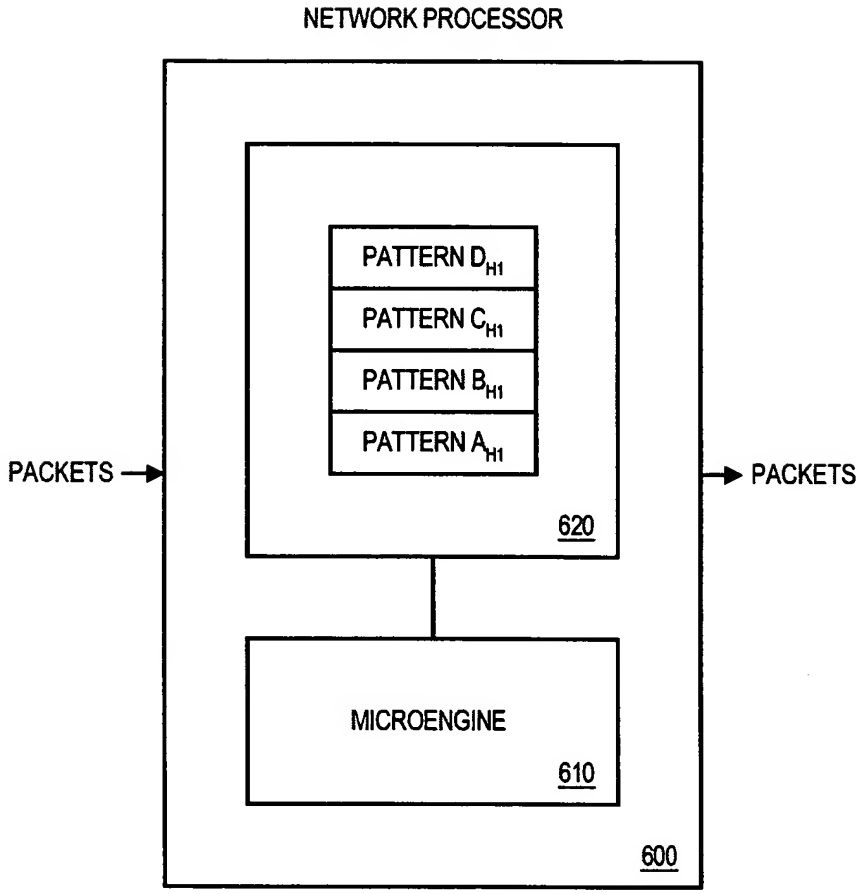
NETWORK PROCESSOR
PACKETS
PACKETS
PATTERN D_{H1}
PATTERN C_{H1}
PATTERN B_{H1}
PATTERN A_{H1}
620
MICROENGINE
610
600

FIG. 6

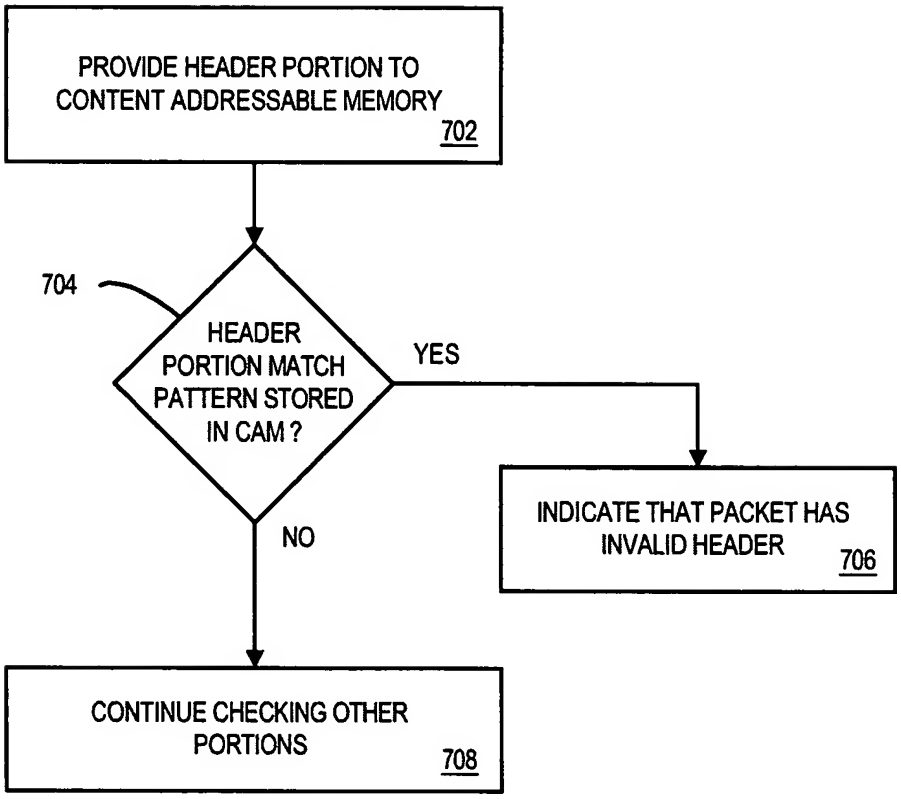
PROVIDE HEADER PORTION TO CONTENT ADDRESSABLE MEMORY
702
704
HEADER PORTION MATCH PATTERN STORED IN CAM ?
YES
NO
INDICATE THAT PACKET HAS INVALID HEADER
706
CONTINUE CHECKING OTHER PORTIONS
708

FIG. 7

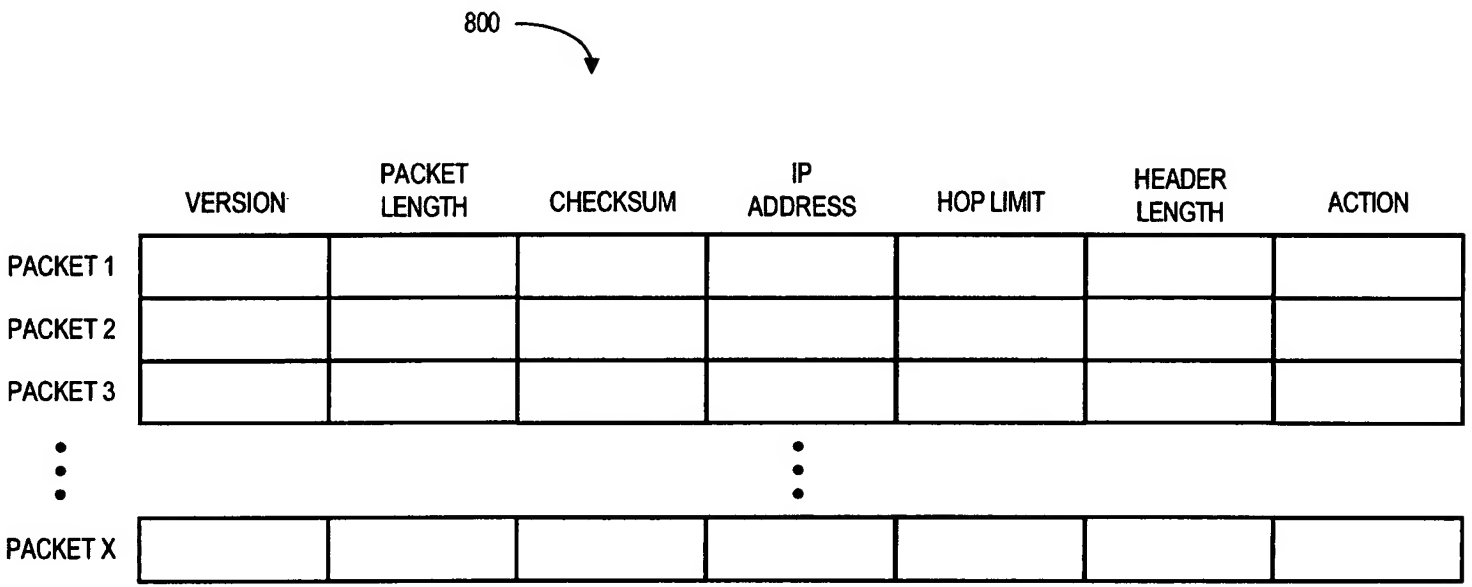
800
VERSION
PACKET LENGTH
CHECKSUM
IP ADDRESS
HOP LIMIT
HEADER LENGTH
ACTION
PACKET 1
PACKET 2
PACKET 3
PACKET X

FIG. 8

900

	VERSION	PACKET LENGTH	CHECKSUM	IP ADDRESS	HOP LIMIT	HEADER LENGTH
PATTERN				0xF		
RELATION				1 (=)		
PATTERN				0xE		
RELATION				1 (=)		
PATTERN				0x7f (127.X.X.X)		
RELATION				1 (=)		
PATTERN				0x (0.X.X.X)		
RELATION				1 (=)		
PATTERN	4	20	0	0xFFFFFFFF	10	5
RELATION	2 (!=)	3 (<)	1 (=)	1 (=)	1 (=)	3 (<)
CHECKS	1	1	1	5	1	1

FIG. 9

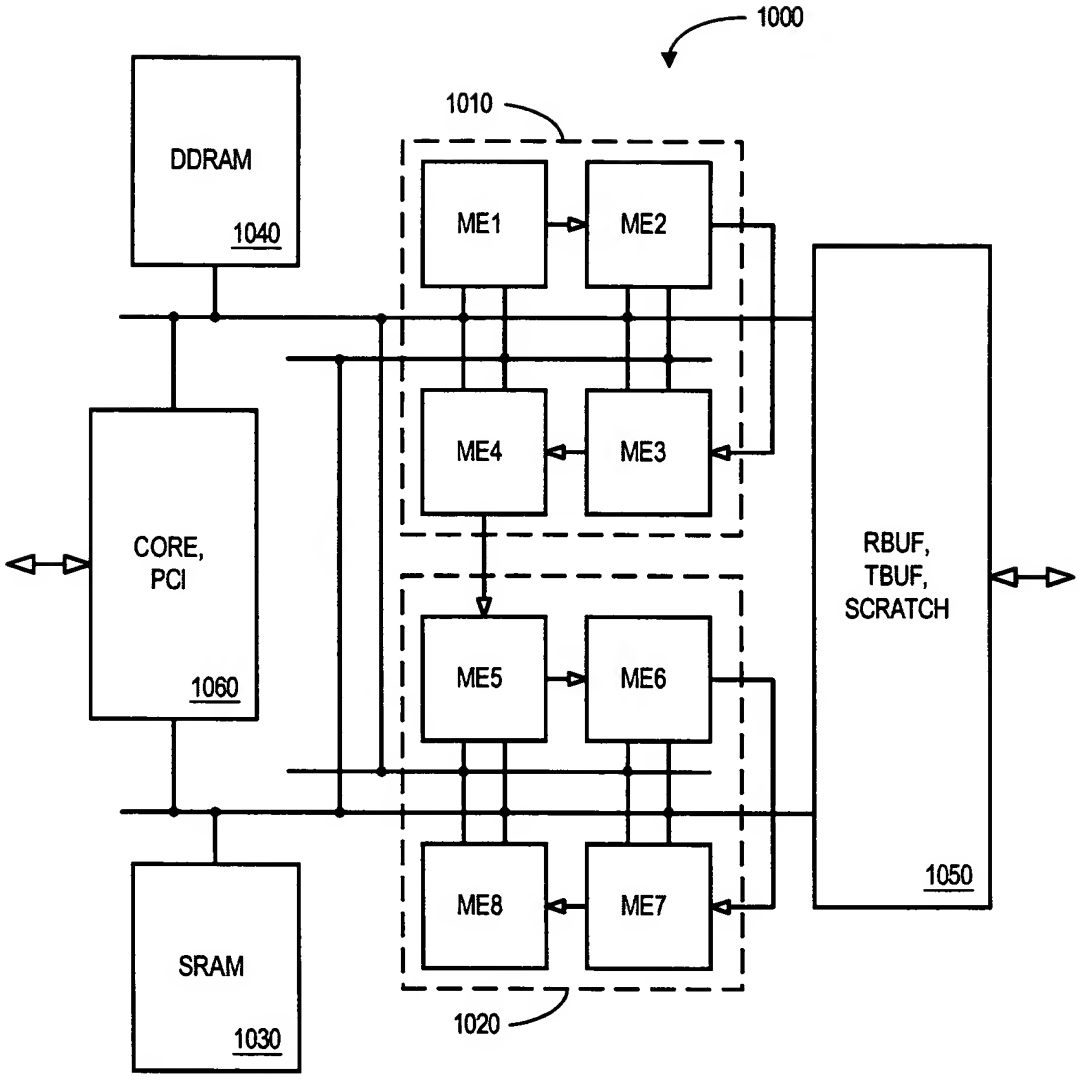
1000
1010
DDRAM
1040
ME1
ME2
ME4
ME3
CORE,
PCI
1060
RBUF,
TBUF,
SCRATCH
1050
ME5
ME6
ME8
ME7
SRAM
1030
1020

FIG. 10

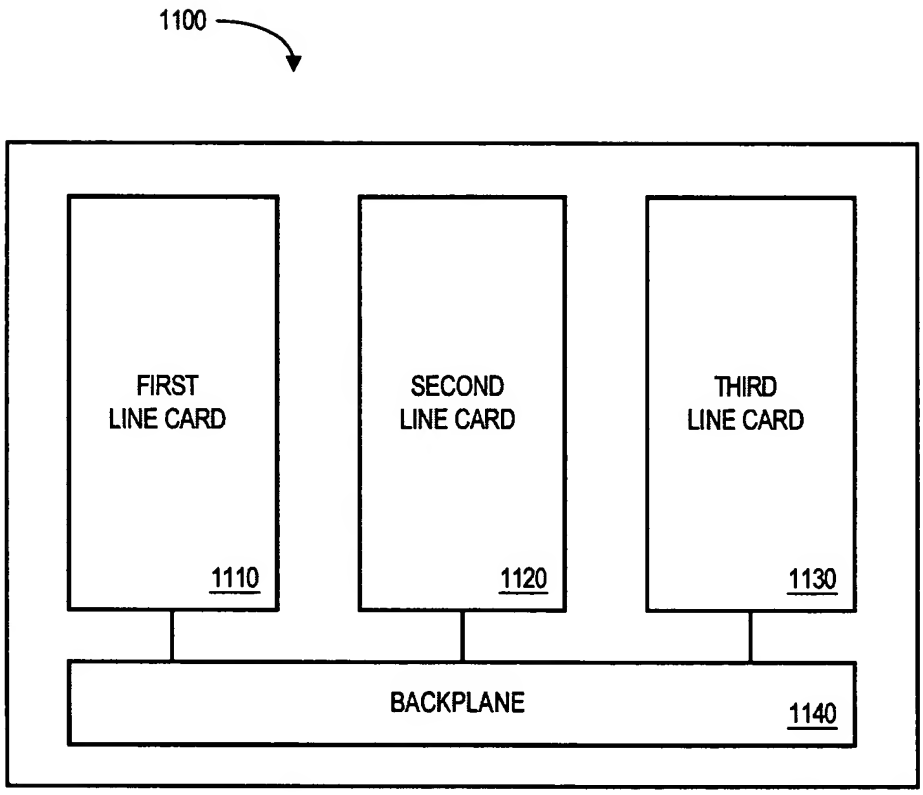
1100
FIRST
LINE CARD
1110
SECOND
LINE CARD
1120
THIRD
LINE CARD
1130
BACKPLANE
1140

FIG. 11